2018-00459 - Multi-clock reconfigurable architectures

Contract type : Public service fixed-term contract
Level of qualifications required : PhD or equivalent
Fonction : Post-Doctoral Research Visit
Level of experience : Recently graduated

Context
In avionic or automotive fields, critical real-time embedded systems coordinate iterative and/or sporadic tasks that may vary during system operation due to external conditions (e.g., flight phases of an airplane, or operation phases of a car...) or internal ones (e.g., example degraded mode). In the end, for some systems, we can imagine hot reconfigurations, motivated by error corrections, changes in their environment, or evolution of functionalities. But these architectural evolutions should be made while preserving security properties linked to the criticality of these systems.

In the particular case of the streamed dataflow model of computation, a higher-order, purely functional domain-specific language such as CAPH has been proposed for programming stream-processing applications on reconfigurable hardware such as FPGAs.

On the other hand, synchronous languages (and among them, Signal), which also allows a design with independent or weakly constrained clocks) make it possible to guarantee security properties in a static architecture framework.

The proposed Post Doctoral aims to take advantage of both the generality of the dataflow model as it is taken into account by CAPH and the properties of the synchronous languages (and in particular Signal) to define a new language, or model, adapted for multi-clock reconfigurable architectures.

This model could be an extension of the polychronous model of the Signal language and of the CCSL standard, allowing a more powerful language than usual Signal, but preserving its safety properties. The designed language or model will be provided with a rich type system including behavioral properties considered as types: refinement types. Its formal (operational) and type semantics will be defined, along with type transformation operations (casting operations in the form of interface synthesis) will be provided.

References


Assignment
Assignments :
The proposed Post Doctoral aims to take advantage of both the generality of the dataflow model as it is taken into account by CAPH and the properties of the synchronous languages (and in particular Signal) to define a new language, or model, adapted for multi-clock reconfigurable architectures.

For a better knowledge of the proposed research subject :
A state of the art, bibliography and scientific references are available at the following URL, do not

General Information
- Theme/Domain : Embedded and Real-time Systems
- Software engineering (BAP E)
- Town/city : Rennes
- Inria Center : CRI Rennes - Bretagne Atlantique
- Starting date : 2018-07-01
- Duration of contract : 1 year, 6 months
- Deadline to apply : 2018-04-30

Contacts
- Inria Team : TEA
- Recruiter : Gautier Thierry / thierry.gautier@inria.fr

Conditions for application
Thank you for applying online

Defence Security :
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST). Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy :
As part of its diversity policy, all Inria positions are accessible to people with disabilities.

Warning : you must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.
hesitate to log in: https://team.inria.fr/tea/

Collaboration:
The recruited person will be in connection with Thierry Gautier who works for Jean-Pierre Talpin.

Main activities
The proposed Post Doctoral aims to take advantage of both the generality of the dataflow model as it is taken into account by CAPH and the properties of the synchronous languages (and in particular Signal) to define a new language, or model, adapted for multi-clock reconfigurable architectures.

Benefits package
- Subsidised catering service
- Partially-reimbursed public transport
- Social security
- Paid leave

Remuneration
Monthly gross salary amounting to 2653 euros