2018-00469 - Automatic parallelization of sparse matrix operations - Post-Doctorant Inria Grenoble Research center

**Contract type:** Public service fixed-term contract  
**Level of qualifications required:** PhD or equivalent  
**Function:** Post-Doctoral Research Visit

### About the research centre or Inria department

Grenoble Rhône-Alpes Research Center groups together a few less than 800 people in 35 research teams and 9 research support departments.

Staff is localized on 5 campuses in Grenoble and Lyon, in close collaboration with labs, research and higher education institutions in Grenoble and Lyon, but also with the economic players in these areas.

Present in the fields of software, high-performance computing, Internet of things, image and data, but also simulation in oceanography and biology, it participates at the best level of international scientific achievements and collaborations in both Europe and the rest of the world.

### Context

The CASH (Compilation and Analysis, Software and Hardware) group works on compilation techniques for high-performance computing. We are currently a team at the LIP laboratory (Lyon), and a subgroup of the ROMA team at Inria.

The overall objective of the CASH team is to take advantage of the characteristics of the specific hardware (generic hardware, hardware accelerators or FPGA) to compile energy efficient software and hardware. The long-term objective is to provide solutions for the end-user developers to use at their best the huge opportunities of these emerging platforms. The research directions of the team are:

- Dataflow models for HPC applications: We target representations that are expressive enough to express all kinds of parallelism and allow further optimizations.
- Compiler algorithms and tools for irregular applications: The extensions of these intermediate representations to enable complex control flow and complex data structures, and the design of associated analysis for optimized code generation for multicore processors and accelerators.
- Compiler Algorithms, Simulation and Tools for Reconfigurable Circuits: The application of the two preceding activities on High Level Synthesis, with additional resource constraints.
- Simulation of Systems on a Chip: A parallel and scalable simulation of Systems-on-Chips, which, combined with the preceding activity, will result in a complete workflow for circuit design.

### Assignment

**Post-doc proposal:**

The polyhedral model [1] allows to represent a set of operations on arrays together with their dependencies. This representation can be used to schedule operations (for example, change the execution order of a set of nested for loops), or to extract parallelism from a sequential program. It has successfully be applied to many matrix-based compute-kernels for aggressive compiler optimization and synthesis of efficient hardware circuits.

A strong limitation, however, is that the model is limited to regular applications: it supports for loops and array accesses, but loop bounds and array indices must be expressible as affine functions of variables and parameters of the compute kernel.

The newly created CASH team works on novel methods to compile and analyze programs and targets in particular hardware generation. One of the research axis is to extend the polyhedral model to irregular applications, e.g. while loops and data-structures other than arrays.

### Main activities

**Objectives of the post-doc:**

- Irregular applications, e.g. while loops and data-structures other than arrays.
- In particular hardware generation. One of the research axis is to extend the polyhedral model to

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**General Information**

- **Theme/Domain:** Distributed and High Performance Computing  
- **Town/city:** Montbonnot  
- **Inria Center:** CRI Grenoble - Rhône-Alpes  
- **Starting date:** 2018-11-01  
- **Duration of contract:** 1 year, 4 months  
- **Deadline to apply:** 2018-04-04

### Contacts

- **Inria Team:** ROMA  
- **Recuriter:** Moy Matthieu / matthieu.moy@inria.fr

### Conditions for application

**Starting date:** 1st November 2018, duration: 16 months.

Applicants should hold a PhD (defended between 1st September 2016 and 31st October 2018) in Systems and Control or Applied Mathematics.

Applications have to be made on-line on the Inria web site before end of March.

**Contact:** Matthieu Moy Matthieu.Moy@univ-lyon1.fr  
http://www.ens-lyon.fr/LIP/CASH/  
https://matthieu-moy.fr/

**Supervisors:**

This post-doc will be supervised by Christophe Alias (Inria Researcher, ENS-Lyon) and Matthieu Moy (Assistant professor, HDR, UCBL).

Christophe Alias http://perso.ens-lyon.fr/christophe.alias/  
's main research topic is hardware compilation in the polyhedral model. He wrote a polyhedral hardware compiler which serves now as a production compiler for the XtremLogic startup (Inria spin-off).

Matthieu Moy https://matthieu-moy.fr/  
's main research area is hardware simulation (using SystemC), on which he has been working for more than 10 years in partnership with STMicroelectronics. More recently, he started working on worst-case execution time for software and worst-case traversal time for networks-on-chip, and compilation for critical systems. He joined the LIP laboratory in 2017 and started working on HLS and polyhedral methods.

**Defence Security:**

This position is likely to be situated in a restricted area (ZRR), as defined in Decree No.
The goal of the post-doc is to study the applicability of polyhedral methods to irregular applications. As a starting point, we will focus on sparse matrices (large matrices containing mostly 0 values, using data-structures that represent only non-zero values).

How does the polyhedral model extend to such applications? In particular how do the notions of iteration domain and affine schedule translate? Which static/dynamic analysis are required? How do the dynamic analysis translate to source code generation?

The goal is to generate process networks corresponding to the input program. This work will be the first building block towards the compilation of hardware for FPGA accelerators. Even though hardware generation itself is out of the scope of the post-doc, the source code generated is expected to fit the input of a C-to-FPGA compiler and to be tested on a FPGA.

Indicative outline:

Here is a more precise list of tasks that could be carried out.

* If needed: study of existing polyhedral techniques for automatic parallelization [1] and related work on parallelization techniques for sparse matrices (for example [2]).

* Study how the shape of sparse matrices [3] can drive the parallelization of simple regular kernels such as matrix sum and matrix multiplication. In these examples, the dependencies between computations are very simple hence polyhedral scheduling and tiling is easier to figure out with sparse matrices.

* Study more complex regular kernels from the Polybench/C suite [4] and propose a parallelization algorithm.

References:

http://dblp.uni-trier.de/rec/bib/reference/parallel/FeautrierL11


http://web.cs.ucla.edu/~pouchet/software/polybench/

Skills

The candidate should have good background in compilation (knowledge of polyhedral methods would obviously be appreciated), and should be familiar with parallel algorithms.

Benefits package

- Subsidised catering service
- Partially-reimbursed public transport
- Social security
- Paid leave
- Flexible working hours
- Sports facilities

Remuneration

Gross salary: 2650 Euros per month