2018-00522 - Energy optimization of synchronous and real-time programs - Post-Doctorant Inria Grenoble Research center

Contract type: Public service fixed-term contract  
Level of qualifications required: PhD or equivalent  
Fonction: Post-Doctoral Research Visit  
Level of experience: Recently graduated

About the research centre or Inria department

Grenoble Rhône-Alpes Research Center groups together a few less than 800 people in 35 research teams and 9 research support departments.

Staff is localized on 5 campuses in Grenoble and Lyon, in close collaboration with labs, research and higher education institutions in Grenoble and Lyon, but also with the economic players in these areas.

Present in the fields of software, high-performance computing, Internet of things, image and data, but also simulation in oceanography and biology, it participates at the best level of international scientific achievements and collaborations in both Europe and the rest of the world.

Context

Over the years, synchronous programming has become a paradigm of choice for real-time embedded systems [1]. For instance, the SCADE commercial tool from Esterel Technologies is the de facto standard in safety critical systems (civil airplanes, trains, subways, nuclear power plants, ...). The benefit of synchronous programming is to precisely control the execution time of the resulting program on the chosen target processor. However, one issue that is not solved is the minimization of the energy consumption, a topic which is becoming more and more important in a large class of embedded systems: satellite systems, portable medical devices, full authority digital engine control (FADEC) in aircraft, and so on. As a consequence, both the execution time and the energy consumption must be minimized for this class of embedded real-time systems.

Dynamic Voltage and Frequency Scaling (DVFS) has emerged as one of the best chip technology to minimize the energy consumption: by lowering the voltage, the dynamic power is reduced, which therefore reduces the overall energy consumption. But at the same time, the frequency must also be lowered, which causes the execution time to increase. We are thus faced with a tradeoff between the energy consumption and the execution time.

The topic of energy minimization for synchronous programs has only recently started to receive attention [2] in the context of the PRET-C synchronous language [3]. In [2], a PRET-C program is first compiled into a so-called Timed Concurrent Control Flow Graph (TCCFG). Each basic block of this TCCFG is then labeled with the number of clock cycles necessary to execute it on the target processor. Finally, executable code is generated from this labeled TCCFG with DVFS switching points inserted at each control point of the TCCFG.

By carefully choosing the (voltage,frequency) values, it is possible to produce schedules of the TCCFG that implement different tradeoffs between the energy consumption and the execution time. In general, two such schedules will be non comparable. E.g., the schedule S1 with execution time 100 and energy 200 cannot be compared with the schedule S2 with execution time 200 and energy 100. In the Pareto sense, we say that S1 does not dominate S2 and that S2 does not dominate S1. In terms of optimization, we are interested in computing the set of schedules that are dominated by no other schedules. These non-dominated schedules are called Pareto optima, and the set of all the Pareto optima is called the Pareto front in the 2D search space (energy, execution time).

Assignment

During the first part of this postdoc, we are interested in improving the technique proposed in [2] so as to generate
better (and even optimal) Pareto fronts, and more importantly to extend it to synchronous programs compiled for multi-core chips and written in ForeC [4].

During the second part of this postdoc, we are interested in the Logical Execution Time paradigm (LET) [5]. The LET abstraction was originally introduced as a real-time programming paradigm and is tightly related to the synchronous model [1]. It has gained traction recently in the automotive industry with the shift to multicore architectures and is now used for development at the ECU level by some OEMs and Tier 1 suppliers [6,7]. Our main objective is to propose new concepts and language constructs for system-level LET that make network communication explicit. This is necessary because network communication does not easily fit into LET intervals. We will apply the proposed methodology to a use case provided by our partner Daimler. An important by-product of this work will be a better understanding of the similarities and differences between the LET and the synchronous models.

References:


Main activities

Main activities:

- Conduct research in collaboration with postdoc advisors.
- Study and review the state of the art.
- Write research articles.
- Attend conferences to present your research results.

Skills

A PhD in formal methods, embedded systems, and/or real-time programming (e.g., analysis, semantics, compiling, code generation, energy optimization, ...). A knowledge of synchronous programming and/or LET would be appreciated.

The working language will be English. French is not a requirement.

Benefits package

- Subsidised catering service
- Partially-reimbursed public transport
- Social security
- Paid leave
- Flexible working hours
- Sports facilities
**Remuneration**
Salary: 2 653 euros gross monthly (about 2.150 euros net).

**General Information**
- **Theme/Domain**: Embedded and Real-time Systems
  Software engineering (BAP E)
- **Town/city**: Montbonnot
- **Inria Center**: CRI Grenoble - Rhône-Alpes
- **Starting date**: 11/1/18
- **Duration of contract**: 1 year, 4 months
- **Deadline to apply**: 3/31/18

**Contacts**
- **Inria Team**: SPADES
- **Recruiter**: Girault Alain / alain.girault@inria.fr

**Conditions for application**
**Starting date**: 1st November 2018.

The postdoc position is for up to 18 months, starting end of 2018 (November ideally). The duration can be between 12 and 18 months.

Applicants should hold a PhD (defended between 1st September 2016 and 31st July 2018) in Systems and Control or Applied Mathematics.

Applications have to be made on-line on the Inria web site before end of March.

Send a CV and the contact information of 2 or 3 recommenders to alain.girault_at_inria.fr and sophie.quinton_at_inria.fr

**Defence Security**:
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST). Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

**Recruitment Policy**:
As part of its diversity policy, all Inria positions are accessible to people with disabilities.

**Warning**: you must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.