2018-00526 - Funded Phd thesis

Level of qualifications required: Graduate degree or equivalent
Function: PhD Position
Level of experience: Recently graduated

About the research centre or Inria department
Grenoble Rhône-Alpes Research Center groups together a few less than 800 people in 35 research teams and 9 research support departments.

Staff is localized on 5 campuses in Grenoble and Lyon, in close collaboration with labs, research and higher education institutions in Grenoble and Lyon, but also with the economic players in these areas.

Present in the fields of software, high-performance computing, Internet of things, image and data, but also simulation in oceanography and biology, it participates at the best level of international scientific achievements and collaborations in both Europe and the rest of the world.

Context
This PhD proposal is already funded by the ANR agency

Location: Lyon, France, LIP Lab

The CASH (Compilation and Analysis, Software and Hardware) group works on compilation techniques for high-performance computing. We are currently a team at the LIP laboratory (Lyon), and a subgroup of the ROMA team at Inria.

The overall objective of the CASH team is to take advantage of the characteristics of the specific hardware (generic hardware, hardware accelerators or FPGA) to compile energy efficient software and hardware. The long-term objective is to provide solutions for the end-user developers to use at their best the huge opportunities of these emerging platforms. The research directions of the team are:

* Dataflow models for HPC applications: We target representations that are expressive enough to express all kinds of parallelism and allow further optimizations.

* Compiler algorithms and tools for irregular applications: The extensions of these intermediate representations to enable complex control flow and complex data structures, and the design of associated analysis for optimized code generation for multicore processors and accelerators.

* Compiler Algorithms, Simulation and Tools for Reconfigurable Circuits: The application of the two preceding activities on High Level Synthesis, with additional resource constraints.

* Simulation of Systems on a Chip: A parallel and scalable simulation of Systems-on-Chips, which, combined with the preceding activity, will result in a complete workflow for circuit design.

Contact: http://www.ens-lyon.fr/LIP/CASH/

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Supervisors:
Laure Gonnord, Associate Professor, HDR. Dr Gonnord is specialized in abstract interpretation and formal methods applied to software design and compilation, with a special focus on scalable techniques.

Lionel Morel, Research Engineer at CEA-List, Grenoble, PhD. Dr Morel has worked for 15 years on programming models and runtimes for dataflow languages and compilation of regular programming structures. Recently he is involved in designing code-generation approaches for the security of embedded applications.

General Information

- Theme/Domain: Distributed and High Performance Computing
- Scientific computing (BAP E)
- Town/city: Lyon
- Inria Center: CRI Grenoble - Rhône-Alpes
- Starting date: 9/1/18
- Duration of contract: 3 years
- Deadline to apply: 3/31/18

Contacts

- Inria Team: ROMA
- Recruiter: Gonnord Laure / laure.gonnord@inria.fr

Conditions for application

Defence Security:
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST). Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy:
As part of its diversity policy, all Inria positions are accessible to people with disabilities.

Warning: you must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.
Assignment

Ph.D proposal:

Scientific context:

After being limited to high-performance computers for a long time, parallel processors have gained wide-spread deployment into the consumer market with the number of cores steadily increasing both in personal computers and smartphones. The problem of high-level code optimization is thus at the heart of program performance not only for scientific applications but also for mainstream, user-centric applications that tend to aggregate and manipulate large amounts of data.

Algorithms manipulating this data are designed using various algorithmic patterns that hopefully express parallelism that can fully exploit the parallelism available on the hardware.

At the heart of HPC and scientific computing applications, a lot of regular algorithms (eg for loops) manipulating regular data structures (eg matrices) have been shown to be optimizable using various compilation techniques. In this context, the polyhedral model [1], a framework introduced in the late eighties, has been successfully applied to a range of the compilation challenges that appear, such as (semi-)automatic parallelization and code generation [2] or data movement optimization.

However, applications today are not limited to regular parallelism: many applications, both in scientific computing and in user-centric context are irregular programs (eg general while loops) that manipulate general data structures (lists, trees, maps).

Parallelizing such irregular programs is an open research problem. The long term objective of the ANR project CODAS (http://codas.ens-lyon.fr) is to address this problem by giving a general framework for reasoning and manipulating programs with general control flow and complex data structures.

The objective of the thesis is to:

Demonstrate that the state-of-the-art methods and tools miss some optimisations opportunities when dealing with irregular control flow (while loops) and data structures other than arrays (lists, trees, maps);

Construct and solve an expressive intermediate representation that captures all data as well as control dependencies, under reasonable assumptions;

Prototype code generation procedure that produces optimized code from this intermediate representation.

A work-in-progress master internship in Spring 2018 will construct the following bases for the Phd:

It will provide a benchmark of interest for the Phd, namely a set of programs to schedule/optimize, middle-sized kernels with code operating on:

Trees (binary trees, general trees): tree traversals, with or without cuts, like *deep learning* or symbolic computing programs;

- Linked lists, maps. Maps are definitely under interest since they are an essential step toward “sparse matrices”, which area common object in scientific computing (numerical simulations).
- It will propose a mini-langage of interest and a way to represent control and data dependencies in a compact way. Formally, we aim to express the notion of dependence, like the “happens-before” relation of the polyhedral model.

References:


Supervisors:

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* Lionel Morel, Research Engineer at CEA-List, Grenoble, PhD. Dr Morel has worked for 15 years on programming models and runtimes for dataflow languages and compilation of regular programming structures. Recently he is involved in designing code-generation approaches for the security of embedded applications.

Keywords:
Compilation, formal methods, parallelism, data-structures, code generation.

Main activities
The Phd will pursue these works in the following directions:

- Consolidate the formal bases: semantics, semantics of dependence, extensions, algorithm to solve the dependences. He might take inspiration from our previous work [3].
- Formulate the legal space of schedules given the program and its dependences.
- Propose a code generation algorithm given a program and its schedule.

All the algorithms and approaches will be implemented and heavily tested to demonstrate both pertinence and scalability.

Skills
Technical skills described in the subject description

Languages: french (B2), english (C1)

Benefits package

- Subsidised catering service
- Partially-reimbursed public transport
- Social security
- Paid leave
- Flexible working hours
- Sports facilities

Remuneration
Gross salary: 1982 euros - 2085 euros