2018-00615 - Research engineer on the verification and evaluation of concurrent architectures.

Level of qualifications required: PhD or equivalent
Function: Temporary scientific engineer

Context
The Institute for Technological Research (IRT) Antoine de Saint Exupéry aims at enforcing the competitiveness of research and industry in Occitanie, Nouvelle Aquitaine, and Provence-Alpes-Côte d'Azur regions in the areas of aeronautics, space, and embedded systems.

Funded at 50% by the public sector and at 50% by the private sector, the IRT gathers the important industry actors of the region working in the above areas, as well as public institutions and their laboratories for working on three strategic technological domains: multifunctional high-performance materials, more electric aircrafts, and embedded systems.

To carry on research and development activities, the IRT seeks a research engineer on the verification and evaluation of concurrent architectures.

Assignment
The CAPHCA (Critical Applications on Predictable High-Performance Computing Architectures) project of the IRT Saint Exupéry uses the objective to design and implement a process enabling a safe exploitation of multi-core hardware architectures and/or modern coprocessors, whilst preserving a high level of performance. The project gathers several industrial partners in the domain of avionics and automotive, providers of simulation technologies for hardware platforms, and the IMC (Interactive Modelling and Cognition) laboratories working in the domain of formal methods, languages, and analysis of real-time systems.

The CAPHCA project started in 2017 for three years, until April 2020.

The current research engineer position holds for 18 months. In this context, the research engineer will be in charge of defining and implementing the methodological and technical means allowing one to:

- Prevent and/or detect errors related to parallelism and concurrency
- Estimate the performance of various architectural solutions, so as to contribute to the guiding the design process towards the optimal solution.

The application domain targets the automotive and avionics critical applications deployed on recent multicore execution platforms (PowerPC, ARM, AUTIX, etc.). These activities will be guided by case studies developed in the framework of the CAPHCA project (representative applications in the domain of avionics and automotive). The methodology will be applied, validated, and evaluated on a subset of these case-studies.

The solutions proposed will rely upon the exploitation of software and/or hardware design models, as well as on formal verification technology, namely the CVPD toolbox developed at INRIA Grenoble (http://cadp.inria.fr/).

Main activities

Activity 1: Verification of OpenMP applications

This activity aims at proposing a tool-supported process enabling one to detect certain classes of errors that may occur on parallel applications described following the OpenMP standard. Two classes of methods will be considered: static analysis methods applied to design models or to code, and dynamic methods based on analysing execution traces. The following tasks will be carried out:

- Formal expression of correctness properties related to parallelism and concurrence (e.g., the data races that may occur in OpenMP applications)
- Study of state-of-the-art methods for detecting errors related to parallelism and concurrence for OpenMP applications

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Activity 2: Estimation of performance

This activity aims at exploiting for performance evaluation purposes some of the notations, tools, and formal models initially used for verification purposes (namely, during the first phase of the project). First, deterministic models will be considered (e.g., for searching the sequence of interactions leading to the worst execution time, highest bus load, etc.), then probabilistic and stochastic models. The work will exploit existing results on the LHT language and the IMM (Interactive Markov Chains) formalism, as well as the classical models, such as DMTMC (Discrete-Time Markov Chains) extended with data values. Quantitative formal models will be constructed by exploiting the whole range of information sources available, such as the measures obtained with the simulators or on the targets. This modelling and evaluation methodology will be sought to be integrated to a design space exploration and optimisation process.

The work will be carried out at IRT Saint Exupéry located in Toulouse (France). It will be co-supervised by the CONVECS project-team of INRIA Grenoble (Mr. Radu Mateescu) and by the CAPHCA project coordinator (Mr. Eric Jenn). INRIA will bring its support, its scientific and technical expertise on formal methods and tools used for the above activities. Besides these specific activities, the research engineer will also contribute to the common objectives of the CAPHCA team:

- Writing project deliverables
- Publishing and/or presenting results in conferences
- Sharing the knowledge

General Information
- Theme/Domain: Embedded and Real-time Systems
- Scientific computing (BAP E)
- Town/City: TOULOUSE
- INRIA Center: CRI Grenoble - Rhône-Alpes
- Starting date: 2018-04-01
- Duration of contract: 1 year, 6 months
- Deadline to apply: 2018-05-31

Contacts
- INRIA Team: CONVECS
- Recruiter: Radu Mateescu / radu.mateescu@inria.fr

About Inria
Inria, the French National Institute for computer science and applied mathematics, promotes “scientific excellence for technology transfer and society.” Graduates from the world’s top universities, Inria’s 2,200 employees rise to the challenges of digital sciences. With its open, agile model, Inria is able to explore original approaches with its partners in industry and academia and provide an efficient response to the multidisciplinary and application challenges of the digital transformation. Inria is the source of many innovations that add value and create jobs.

The keys to success
Holder of a PhD on one or more of the areas covered by the job (parallel programming using OpenMP, formal verification by model checking, modelling and performance analysis, concurrent architectures, etc.).

Conditions for application

Defence Security:
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1452 relating to the protection of national scientific and technical potential (PPST). Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy:
As part of its diversity policy, all Inria positions are accessible to people with disabilities.

Warning: you must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.
Skills

Required skills and knowledge:

- Parallel programming (in particular using OpenMP)
- Ideally, formal modelling for verification purposes (expression of properties, behavioural description, etc.).
- Practical experience involving the above topics

Required aptitudes:

- Curiosity, autonomy, communication capabilities (oral and written)
- Interest for the concrete usage of technologies (in particular, software development)