2018-00852 - Hardware control techniques for tight worst-case execution times (WCETs) on many-core architectures

Level of qualifications required: PhD or equivalent
Function: Post-Doctoral Research Visit
Level of experience: From 3 to 5 years

About the research centre or Inria department
The Inria Rennes - Bretagne Atlantique Centre is one of Inria's eight centres and has more than thirty research teams. The Inria Center is a major and recognized player in the field of scientific research in the heart of a rich R&D and innovation ecosystem: highly innovative PMEs, large industrial groups, competitiveness clusters, research and higher education players, laboratories of excellence, technological research institute, etc.

Context
Scientific context
Safety-critical systems (e.g. aviation, medical devices, automotive, ...) have so far used simple uni-core hardware systems in order to control their predictability, in order to meet timing constraints. Still, many critical embedded systems have increasing demand in computing power, and simple uni-core processors are not sufficient anymore. General-purpose multi-core processors are not suitable for safety-critical real-time systems, because they include complex micro-architectural elements (cache hierarchies, branch, stride and value predictors) that mean to improve average-case performance, and for which worst-case performance (worst-case execution times, WCET) is difficult to predict.

Some architectures were designed with both performance and predictability in mind, and are good candidates to run critical real-time software. Examples of such architectures are the Kalray MPPA many-core architecture (http://www.kalrayinc.com/) or the Recover many-core hardware (http://www.recover.systems/).

Keywords
Compilers, Real-time, Multi-core, Computer architecture, Worst-case execution time estimation

Involved groups
The post-doc will be supervised by people from the PACAP group (Isabelle Puaut) and the Cairn group (Steven Derrien)

Assignment
The objective of this postdoc position will be to design and implement techniques, enabling the calculation of tight Worst-Case Execution Time (WCET) estimates on many-core architectures. Proposed techniques will optimize existing mapping/scheduling techniques to better control the hardware with the objective of reducing the WCET estimate of parallel applications. In particular, special attention will be paid to the reduction of interference on shared resources (bus access, memory banks, NoC) and management of the hierarchy (on-chip memory and caches). Among others, we foresee two research directions that look promising, not yet fully explored in the literature:

- Automatic mapping of data structures on memory banks to avoid contentions
- Configuration of Network on Chip (NoC) to reduce data transfer time (e.g. application specific routing, static calculation of TDMA slots to reduce worst-case end-to-end data transfer latency)

The supervisors will be members of the Pacap and Cairn research groups (Pacap for expertise on WCET computation, computer architecture and compilers, Cairn for automatic parallelization, computer architecture and compilers). The techniques developed by the postdoc will be experimented on the architectures and tools available in the Cairn and Pacap groups and within the H2020 Argo project (e.g. GeCos source-to-source optimization environment, Heptane WCET estimation tool, mapping and scheduling tools developed in both groups).

References

Main activities
The successful candidate will engage in explorative scientific research in the field of decentralized control techniques for tight worst-case execution times (WCETs) on many-core architectures.
systems and algorithms, with focus on browser-based deployment and application.

Skills
- Ability to conduct research autonomously in a collaborative setting.
- Self-initiative, curiosity and experimental rigor.
- Excellent ability to express oneself clearly and convincingly in both written and oral English.
- A genuine drive to expand one's knowledge and horizons.
- Excellent experimental and programming skills.
- A good grasp of current research questions in distributed systems and/or distributed algorithms research.

Benefits package
- Subsidised catering service
- Partially-reimbursed public transport

Remuneration
Post-doc: monthly gross salary amounting to 2653 euros