### 2018-01027 - Scheduling, mapping and code generation of partially expanded dataflow graphs

**Contract type:** Public service fixed-term contract  
**Renewable contract:** Oui  
**Level of qualifications required:** PhD or equivalent  
**Function:** Post-Doctoral Research Visit

#### About the research centre or Inria department
The Inria Rennes - Bretagne Atlantique Centre is one of Inria’s eight centres and has more than thirty research teams. The Inria Center is a major and recognized player in the field of digital sciences. It is at the heart of a rich R&D and innovation ecosystem: highly innovative PMEs, large industrial groups, competitiveness clusters, research and higher education players, laboratories of excellence, technological research institutes, etc.

#### Context
The goal of this post-doctorate is to participate in a project to develop a scheduler synthesis tool suite that exploits partial expansion graphs (PEG) and affine dataflow graphs (ADFG) to generate efficient schedules of real-time parallel applications on many-core architectures. Starting from the initial implementation of an application modeled as a synchronous data flow graph with parameterized actors, we will investigate implementations using parameterized graphs and/or code generation techniques.

The ADFG tool will then be used to compute the scheduling and mapping of the implemented application. Scheduling and mapping will require us to investigate open problems such as shared memory access contentions and optimal FIFO channel allocations. The scheduler will be either time-triggered or deferred to the application implementation (ASAP, RM or DM). A timing analysis case study will additionally be performed by a profiling tool (e.g., valgrind) and/or the WCET analysis tool Heptane of the Inria PACAP team.

#### Assignment
Candidates must have a strong and demonstrated background in scheduling analysis and RTES design, synchronous, cyclo-static dataflow and Kahn process networks, WCET analysis and profiling as well as C and Java programming. Knowledge and experience of PEG and familiarity with the ADFG tool and the DSPCAD framework (DIF-GPU, DICE and LIDE) will be plusses.

The successful applicant will join Inria project team TEA (with benefits according to Inria salary and social benefits standards) and participate to an ongoing project in collaboration with the University of Maryland. The initial appointment will be of ten month and possibly renewed in the context of an upcoming Insa-IETR-Inria Chair.

For a better knowledge of the proposed research subject:

- **References**
  https://link.springer.com/referenceworkentry/10.1007%2F978-94-017-7267-9_9
  2. ADFG: affine data-flow graphs  
  http://polychrony.inria.fr/ADFG
  3. Partial Expansion Graphs: Exposing Parallelism and Dynamic Scheduling Opportunities for DSP Applications  
  https://ieeexplore.ieee.org/document/6341457
  4. Handbook of signal processing systems  

- **Collaboration**
  Jean-Pierre Talpin, Thierry Gautier (@inria.fr), Hai-Nam Tran (@univ-brest.fr)

#### Main activities
The goal of this post-doctorate is to participate in a project to develop a scheduler synthesis tool suite that exploits partial expansion graphs (PEG) and affine dataflow graphs (ADFG) to generate efficient schedules of real-time parallel applications on many-core architectures. Starting from the initial implementation of an application modeled as a synchronous data flow graph with parameterized actors, we will investigate implementations using parameterized graphs and/or code generation techniques.

#### Benefits package
- Subsidised catering service
- Partially-reimbursed public transport

#### Remuneration
Monthly gross salary amounting to 2653 euros.

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#### About Inria
Inria, the French national research institute for the digital sciences, promotes scientific excellence and technology transfer to maximise its impact. It employs 2,400 people. Its 200 agile project teams, generally with academic partners, involve more than 3,000 scientists in meeting the challenges of computer science and mathematics, often at the interface of other disciplines. Inria works with many companies and has assisted in the creation of over 160 startups. It strives to meet the challenges of science, society and the economy.

#### Conditions for application
Please submit online: your resume, cover letter and letters of recommendation eventually.

For more information, please contact jean-pierre.talpin@inria.fr

**Defence Security:**
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST). Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

**Recruitment Policy:**
As part of its diversity policy, Inria positions are accessible to people with disabilities.

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**Warning:** You must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.