2018-01027 - Scheduling, mapping and code generation of partially expanded dataflow graphs

**Contract type**: Public service fixed-term contract  
**Renewable contract**: Oui  
**Level of qualifications required**: PhD or equivalent  
**Fonction**: Post-Doctoral Research Visit

**About the research centre or Inria department**

The Inria Rennes - Bretagne Atlantique Centre is one of Inria's eight centres and has more than thirty research teams. The Inria Center is a major and recognized player in the field of digital sciences. It is at the heart of a rich R&D and innovation ecosystem: highly innovative PMEs, large industrial groups, competitiveness clusters, research and higher education players, laboratories of excellence, technological research institute, etc.

**Context**

The goal of this post-doctorate is to participate in a project to develop a scheduler synthesis toolsuite that exploits partial expansion graphs (PEG) and affine dataflow graphs (ADFG) to generate efficient schedules of real-time parallel applications on many-core architectures. Starting from the initial implementation of an application modeled as a synchronous data flow graph with parameterized actors, we will investigate implementations using parameterized graphs and/or code generation techniques.

The ADFG tool will then be used to compute the scheduling and mapping of the implemented application. Scheduling and mapping will require us to investigate open problems such as shared memory access contentions and optimal FIFO channel allocations. The scheduler will be either time-triggered or deferred to the application implementation (ASAP, RM or DM). A timing analysis case study will additionally be performed by a profiling tool (e.g., valgrind) and/or the WCET analysis tool Heptane of the Inria PACAP team.

**Assignment**

Candidates must have a strong and demonstrated background in scheduling analysis and RTES design, synchronous, cyclo-static dataflow and Kahn process networks, WCET analysis and profiling as well as C and Java programming. Knowledge of PEG and familiarity with the ADFG tool and the DSPCAD framework (DIF-GPU, DICE and LIDE) will be pluses.

The successful applicant will join Inria project-team TEA (with benefits according to Inria salary and social benefits standards) and participate to an ongoing project in collaboration with the University of Maryland. The initial appointment will be of ten month and possibly renewed in the context of an upcoming Insa-IETR-Inria Chair.

**For a better knowledge of the proposed research subject:**

**References**

https://link.springer.com/referenceworkentry/10.1007%2F978-94-017-7267-9_36


[3] Partial Expansion Graphs: Exposing Parallelism and Dynamic Scheduling Opportunities for DSP Applications  
https://ieeexplore.ieee.org/document/6341457


**Collaboration**

Jean-Pierre Talpin, Thierry Gautier (@inria.fr) Hai-Nam Tran (@univ-brest.fr)

**Main activities**

The goal of this post-doctorate is to participate in a project to develop a scheduler synthesis toolsuite that exploits partial expansion graphs (PEG) and affine dataflow graphs (ADFG) to generate efficient schedules of real-time parallel applications on many-core architectures. Starting from the initial implementation of an application modeled as a synchronous data flow graph with parameterized actors, we will investigate implementations using parameterized graphs and/or code generation techniques.

**Benefits package**

- Subsidised catering service
- Partially-reimbursed public transport

**Remuneration**
monthly gross salary amounting to 2653 euros

General Information

- **Theme/Domain**: Embedded and Real-time Systems
  Scientific computing (BAP E)
- **Town/city**: Rennes
- **Inria Center**: CRI Rennes - Bretagne Atlantique
- **Starting date**: 2018-10-01
- **Duration of contract**: 10 months
- **Deadline to apply**: 2018-11-30

Contacts

- **Inria Team**: TEA
- **Recruiter**: Talpin Jean-pierre / jean-pierre.talpin@inria.fr

About Inria

Inria, the French National Institute for computer science and applied mathematics, promotes “scientific excellence for technology transfer and society”. Graduates from the world’s top universities, Inria’s 2,700 employees rise to the challenges of digital sciences. With its open, agile model, Inria is able to explore original approaches with its partners in industry and academia and provide an efficient response to the multidisciplinary and application challenges of the digital transformation. Inria is the source of many innovations that add value and create jobs.

Conditions for application

Please submit online: your resume, cover letter and letters of recommendation eventually

For more information, please contact jean-pierre.talpin@inria.fr

Defence Security:

This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST). Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy:

As part of its diversity policy, all Inria positions are accessible to people with disabilities.

**Warning**: you must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.