Offer #2019-01682

PhD Position F/M Multi-technologies on-chip interconnects for manycore architectures

Contract type : Fixed-term contract

Level of qualifications required : Graduate degree or equivalent

Fonction : PhD Position

Context

Within the framework of a partnership public with French National Research Agency (ANR): ANR Project SHNoC

Since few years we are witnessing the emergence of manycore architectures, namely to the implementation of massive parallelism on a single chip. Associated with the shrinking size of the transistors, announced reaching an 11nm technology on 2020, these manycore architectures should reach the integration of thousands of heterogeneous cores allowing huge parallel computation capabilities suitable for High Performance Computing (HPC) and embedded systems.

These parallelism capabilities obviously generate an enormous amount of data exchanges making the communication medium a key element of the overall performance of the system. Massively parallel manycore architectures are showing the scalability limits of electrical NoCs (ENoCs) that suffer when facing thousands of cores. This generates an increase in the latency, hence in the power consumption. Theses degradations are also amplified while the size of the wire decreases.

Technology evolution has allowed for the integration of silicon photonics and wireless on- chip communications, creating Optical and Wireless NoCs (ONoCs and WNoCs, respectively) paradigms. The recent publications highlight advantages and drawbacks for each technology: WNoCs are efficient for broadcast, ONoCs have low latency and high integrated density (throughput/cm2) but inefficient in multicast, and ENoC still efficient for average size of NoC. In this context, this project proposes to associate these three technologies. Each NoC technology possesses particular and complementary advantages allowing to efficiently route messages depending on their profile: short or long distance, uni- or multi-cast.

Assignment

The main objectives of this thesis are:

- Defining a Scalable Hybrid NoC (SHNoC) associating electric, optic and wireless communication NoCs to take advantage of each technology;
- Provide adaptive Quality of Service by efficiently routing the messages on the most efficient technology with respect to application constraints (e.g. minimizing energy, respecting latency, etc.).

Main activities

The thesis works will be organized regarding the following activities:

- The first activity consists in the study of the state of the art in recent advances for each on-chip interconnect technology. This study will allow to identify the process compatibilities and the physical possibilities or limitations of association (e.g. number of antennas that is physically possible to implement on a specific chip size).
- The second activity is the characterization of communication models (energy, throughput, latency) for each NoC technology. The aim is to define high level models to integrate them in a manycore simulator (e.g. NoXiM) in order to evaluate communication performance on real life benchmark.
- Regarding the last activity, we will propose routing protocols to provide a Quality of Service (QoS) to the application by targeting a minimal energy consumption, or latency. This routing protocol will define, regarding the targeted QoS and the message profile, the path among the hybrid interconnect.

Skills

- Master student in computer science

- Knowledges and skills in

embedded digital architectures, parallel computing

coding in SystemC, C++, Python, VHDL/HLS, Matlab

- Knowledge in on-chip interconnects, and in optical and wireless communications is a plus but is not mandatory.

Benefits package

- Partial reimbursement of public transport costs
- Professional equipment available (videoconferencing, loan of computer equipment, etc.)
- Social, cultural and sports events and activities
- Access to vocational training
- Social security coverage

General Information

- **Theme/Domain :** Architecture, Languages and Compilation
  IT Technical and production engineering (BAP E)
- **Town/city :** Lannion
- **Inria Center :** Centre Inria de l'Université de Rennes
- **Starting date :** 2019-11-01
- **Duration of contract :** 3 years
- **Deadline to apply :** 2019-06-30

Contacts

- **Inria Team :** CAIRN
- **PhD Supervisor :**
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About Inria

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The keys to success

There you can provide a "broad outline" of the collaborator you are looking for what you consider to be necessary and sufficient, and which may combine :

- tastes and appetencies,
- area of excellence,
- personality or character traits,
- cross-disciplinary knowledge and expertise...

This section enables the more formal list of skills to be completed and 'lightened' (reduced) :

- "Essential qualities in order to fulfil this assignment are feeling at ease in an environment of scientific dynamics and wanting to learn and listen."
- " Passionate about innovation, with expertise in Ruby on Rails development and strong influencing skills. A thesis in the field of **** is a real asset."

Warning : you must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.

Instruction to apply

Defence Security :
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST).Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy :
As part of its diversity policy, all Inria positions are accessible to people with disabilities.