Offer #2022-04361

RISC-V Multicore Processor Design and Specialization

Contract type : Fixed-term contract

Level of qualifications required : Graduate degree or equivalent

Fonction : Temporary scientific engineer

About the research centre or Inria department

The Inria Rennes - Bretagne Atlantique Centre is one of Inria's eight centres and has more than thirty research teams. The Inria Center is a major and recognized player in the field of digital sciences. It is at the heart of a rich R&D and innovation ecosystem: highly innovative PMEs, large industrial groups, competitiveness clusters, research and higher education players, laboratories of excellence, technological research institute, etc.

Context

Host team: The project will be held in the TARAN (formerly CAIRN) team of the IRISA/INRIA laboratory. The TARAN team, with more than 35 members from Inria, UR1, and ENS Rennes, has participated in several national and European R&D projects (H2020 ARGO, FP7 Alma, FP7 Flextiles) and has strong industrial collaborations (e.g., Safran, Thales, Alcatel, Orange, STMicroelectronics, Technicolor, and various SMEs). TARAN has recognized experience in several domains related to the project, such as embedded system design, fault tolerance, safety-critical systems, computing architectures, design tools for specialized hardware architectures.

Acquiring new skills: As a new member of the TARAN team, you will be integrated in a research group with excellent prestige and deep knowledge of embedded systems. The TARAN research group can provide you with a more solid understanding and knowledge of computer architectures and hardware design. For instance, the host team has high-quality papers published using RISC-V-based processors and dedicated hardware designs, subjects that you will be able to learn much more about and increase my background in this area.

Main activities

Position: Research Engineer/Research Associate

Keywords: processor architecture, multicore, hardware accelerator, high-level synthesis, FPGA design, RISC-V

RISC-V is a free, open, and extensible Instruction-Set Architecture (ISA) for programmable processor design that is straightforward to implement in many microarchitectural styles [2]. Unlike many earlier efforts that designed open processor cores, RISC-V is an ISA specification, intended to allow many different hardware implementations to leverage common software development. RISC-V is a modular architecture, with variants covering 32/64/128-bit address spaces [2]. The base integer instruction set is lean, requiring fewer than 50 user-level hardware instructions to support a full modern software stack, which enables microprocessor designers to quickly bring up fully functional prototypes and add additional features incrementally. RISC-V comes with several open-source tools, such as a compiler, several simulators, and Linux distributions. Different implementations as soft cores are already available as RTL source code or through code generation [4][5].

In addition to simplifying the implementation of new microarchitectures, the RISC-V design provides an ideal base for building custom accelerators [3]. Accelerators can reuse common processor implementations and they can share a single software stack, including the compiler toolchain and operating system binaries. This dramatically reduces the cost of designing and bringing up custom accelerators. Finally, RISC-V is also suitable for multicore implementation, especially following shared-memory multiprocessor architectures.

In the Inria/IRISA/Taran team, we are currently designing an in-order core micro-architecture supporting 32-bit RISC-V instruction set [5][6]. The Comet core is designed from C++-based specifications using High-Level Synthesis (HLS) tools. The design is compatible with Catapult Synthesis from Mentor Graphics targeting a 28nm CMOS technology library (gate synthesis and validation with Synopsys Design Compiler and Modelsim) and with Xilinx VivadoHLS for FPGA prototyping. Synthesis results obtained through HLS show similar or better performance (clock frequency, area, power, execution time of benchmarks) than other open-source processor core designs [4].

The subject of this work is to extend the Comet processor towards a shared-memory multicore architecture. The main challenge is to deal with C++-based specification of cache memory, on-chip

interconnect, protocols for shared memory and multicore specifications. In particular, the research question is how to specify such complex parallel computing pipelines with high-level synthesis technology and to demonstrate that there is a potential high gain in design time without jeopardizing performance and cost (which was the case for the one-core).

In this work, we will also study how some C++-based hardware accelerators (FPU [3], vector extensions, FFT core, approximate arithmetic operators, etc.) can be build and coupled to the RISC-V multicore architecture.

We also have several applications of this core in the context of fault tolerance (space, avionics) and hardware security. If relevant, the recruited person can also contribute to projects related to this area.

References

[1] A. Waterman et al., The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Version 2.0, tech. report UCB/EECS-2014-54, EECS Dept., UC Berkeley, May 2014.

[2] K. Asanovic and D.Patterson, “The Case for Open Instruction Sets,” Microprocessor Report, Aug. 2014.

[3] V. Patil et al., “Out of Order Floating Point Coprocessor for RISC-V ISA,” Proc. 19th Int’l Symp. VLSI Design and Test, 2015.

[4] https://github.com/chipsalliance/rocket-chip

[5] S. Rokicki, D. Pala, J. Paturel, and O. Sentieys. What You Simulate Is What You Synthesize: Designing a Processor Core from C++ Specifications. In 38th IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pages 1–8, Nov. 2019.

[6] https://gitlab.inria.fr/srokicki/Comet

Skills

The recruited person is expected to develop complex processor architectures leveraging C++ and High-Level Synthesis. We also expect to have prototype implementations of the developed techniques on FPGA and ASIC.

Desired skills include:

- Computer architecture, hardware design, VLSI circuit design.

- Basic knowledge in compilers.

- Familiarity with the C/C++ language or other languages.

- Familiarity with FPGA/ASIC design and/or High-Level Synthesis.

- Optimization methods

Mostly importantly, we seek highly motivated and active researchers.

Benefits package

- Subsidized meals
- Partial reimbursement of public transport costs

Remuneration

monthly gross salary from 2562 euros according to diploma and experience

General Information

- **Theme/Domain :** Architecture, Languages and Compilation
- **Town/city :** Rennes
- **Inria Center :** Centre Inria de l'Université de Rennes
- **Starting date :** 2022-02-01
- **Duration of contract :** 2 years
- **Deadline to apply :** 2022-09-30

Contacts

- **Inria Team :** TARAN
- **Recruiter :**

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About Inria

Inria is the French national research institute dedicated to digital science and technology. It employs 2,600 people. Its 200 agile project teams, generally run jointly with academic partners, include more than 3,500 scientists and engineers working to meet the challenges of digital technology, often at the interface with other disciplines. The Institute also employs numerous talents in over forty different professions. 900 research support staff contribute to the preparation and development of scientific and entrepreneurial projects that have a worldwide impact.

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Instruction to apply

Please submit online : your resume, cover letter and letters of recommendation eventually

For more information, please contact olivier.sentieys@inria.fr

Defence Security :
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST).Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy :
As part of its diversity policy, all Inria positions are accessible to people with disabilities.