Informations générales

- Thème/Domaine : Calcul distribué et à haute performance
- Centre Inria : CRI Grenoble - Rhône-Alpes
- Date limite pour postuler : 01-05-2018
- Durée de contrat : 3 ans
- Date de prise de fonction souhaitée : 01-10-2018

Contacts

- Equipe Inria : ROMA
- Recruteur : Moy Matthieu / matthieu.moy@inria.fr

Conditions pour postuler

The campaign is not open to local students who have not done any significant mobility.

Sécurité défense :
Ce poste est susceptible d’être affecté dans une zone à régime restrictif (ZRR), telle que définie dans le décret n°2011-1425 relatif à la protection du potentiel scientifique et technique de la nation (PPST). L’autorisation d’accès à une zone est délivrée par le chef d’établissement, après avis ministériel favorable, tel que défini dans l’arrêté du 03 juillet 2012, relatif à la PPST. Un avis ministériel défavorable pour un poste affecté dans une ZRR aurait pour conséquence l’annulation du recrutement.

Politique de recrutement :
Dans le cadre de sa politique diversité, tous les postes Inria sont accessibles aux personnes en situation de handicap.

Attention : Les candidatures doivent être déposées en ligne sur le site Inria. Le traitement des candidatures adressées par d'autres canaux n'est pas garanti.
acceptable. Most gains in performance now come from the augmentation of the
number of computation units (processor cores, specialized processors). New
programming paradigms have to be found to continue increasing performance in a
given energy budget.

One solution is to implement the main algorithms of a computation in hardware, and
map it to reconfigurable circuits (FPGA, Field Programmable Gate Array) [2]. To
execute an application on FPGA, new technological locks must be overcome. Among
them is the automatic and efficient translation of an algorithm into a circuit design.
This operation is called HLS (High-level synthesis).

Translating a program into a circuit is done in several steps. First, the front-end
generates an intermediate representation adapted to circuit synthesis. In the tools
developed by CASH, this formalism is called “Data-aware Process Network” (DPN)
and represents a network of processes that captures the parallelism of an application
and the communications between parallel processes. Then, the back-end translates
each component of the process network into hardware while ensuring a good reuse of
hardware resources. In the end, the circuit can be seen as a very large network of
pipelined processes, reading inputs and producing outputs periodically.

The newly created CASH (http://www.ens-lyon.fr/LIP/CASH/) team works on novel
approaches to extract parallelism from an imperative program to an intermediate
representation. To evaluate the quality and correctness of the generated process
network, one option is to execute them, either by simulating them or by running them
through the back-end and execute the result on an FPGA. However, this would not
provide strong correctness guarantees, just like testing software doesn’t prove its
correctness.

Principales activités

Objectives of the Thesis:

The overall objective of the thesis is to explore the possibilities of formal verification
of DPN (Data-aware Process Networks). The main technique we envision is model-
checking, i.e. exploration of the state-space.

The first step is to connect to existing verification tools. A good candidate is the CADP
toolchain (http://cadp.inria.fr/), developed at Inria by the CONVECS team. This
connection can take the form of a compiler that reads DPNs and produces the input
format for CADP (LOTOS, or some lower-level formalism like AUT or BCG).

Once a basic connection is done, we can start verifying properties on the generated
automata, like absence of deadlocks, temporal logic properties, or equivalence with a
reference automaton.

The particular structure of DPN (static control, lot of FIFO-based communication)
should make model-checking easier. For example, we expect partial-order reduction
techniques to be very efficient on DPN.

The next steps of the Ph.D will therefore be to apply reduction techniques to make
the verification scale to large DPN. Many techniques are already implemented in
model-checking tools like CADP, and new techniques may be proposed as part of the
Ph.D.

Another direction to explore is the feedback we can get from verification, in particular
when the verification fails. Typical model-checkers provide a counter-example (a trace
violating the property) in this case, but we can use the information provided by the
model-checker to get a better diagnosis (e.g. notice that the verification failed
because of an incorrect channel dimensioning, or because the execution order is
wrong) and ideally suggest a fix.

Compétences

Expected skills:

The candidate should have good background in compilation. A good knowledge of
parallel programming, both from the practical point of view and from the formal point
of view (semantics, state-machine, ...) is required. Prior experience with model-
checking is obviously appreciated. The Ph.D consists in theoretical aspects and
practical ones, hence the candidate should have both a good theoretical background
and good programming skills.

References:

[1] Haron, Nor Zaidi and Hamdioui, Said Why is CMOS scaling coming to an END?,
Design and Test Workshop, 2008. IDT 2008. 3rd International

[2] Altera Corporation Altera FPGAs Achieve Compelling Performance-per-Watt in
Cloud Data Center Acceleration Using CNN Algorithms
Supervisors:

This thesis will be supervised by Christophe Alias (Inria Researcher, ENS-Lyon) and Matthieu Moy (Assistant professor, HDR, UCBL).

Christophe Alias (http://perso.ens-lyon.fr/christophe.alias/)’s research interests includes automatic parallelization, polyhedral compilation and high-level synthesis for FPGA circuits. He wrote a process-network compiler that he transferred to the Xtremlogic startup.

Matthieu Moy (https://matthieu-moy.fr)’s main research area is hardware simulation (using SystemC) and formal verification (model-checking, abstract interpretation, SMT solving). More recently, he started working on worst-case execution time for software and worst-case traversal time for networks-on-chip, and compilation for critical systems. He joined the LIP laboratory in 2017 and started working on HLS and polyhedral methods.

Keywords:

Compilation, model-checking, formal methods, parallelism, high-level synthesis.

Avantages sociaux

- Subsidised catering service
- Partially-reimbursed public transport
- Social security
- Paid leave
- Flexible working hours

Rémunération


Monthly salary after taxes: around 1596,05€ for 1st and 2nd year. 1678,99€ for 3rd year. (medical insurance included).