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Contexte et atouts du poste
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Mission confiée
The PhD Thesis will be funded by Inria.

Objectives of the PhD Thesis

With this thesis, we want to conduct a thorough analysis of reduced numerical precision training of DL systems. We plan to do this at two levels: arithmetic (use appropriate numerical formats and bit widths for all the computations used during training) and algorithmic (by attempting to improve the practical convergence properties of the optimization procedures used to train neural networks).

A first objective is for the PhD student to build/extend a deep learning platform with custom precision arithmetic. This will require building customized floating-point operators down to very few bits of exponent and mantissa which offer a desirable balance between accuracy and energy efficiency. In parallel, the plan is to investigate how mixed precision support (i.e., hard-ware support for several numeric formats with varying costs and accuracies) during successive iterations of the SGD training algorithm impacts accuracy and performance.

With respect to existing works that generally consider predefined numeric formats, our aim is to do a more in-depth analytical design space exploration by looking at the entire spectrum of low precision numbers.

Informations générales

- **Thème/Domaine:** Architecture, langages et compilation
- **Système & réseaux (BAP E)**
- **Ville:** Rennes
- **Centre Inria:** CRI Rennes - Bretagne Atlantique
- **Date de prise de fonction souhaitée:** 2020-10-01
- **Durée de contrat:** 3 ans
- **Date limite pour postuler:** 2020-05-12

**Contacts**

- **Equipe Inria:** CRAIN
- **Directeur de thèse:** Sentieys Olivier / Olivier.Sentieys@inria.fr

**Principal activités**

Context of the PhD Thesis

Deep Learning is one of the most intensively and widely used predictive models in the field of Machine Learning. Convolutional Neural Networks (CNNs) [7] have shown to achieve state-of-the-art accuracy in computer vision [6], and have even surpassed the error rate of the human visual cortex. These neural network techniques have quickly spread beyond computer vision to other domains. For instance, deep CNNs have revolutionized tasks such as face recognition, object detection, and medical image processing. Recurrent neural networks (RNNs) achieve state-of-the-art results in speech recognition and natural language translation [1], while ensembles of neural networks already offer superior predictions in financial portfolio management, playing complex games [9] and self-driving cars [2].

Despite the benefits that DL brings to the table, there are still important challenges that remain to be addressed if the computational workloads associated with NNA are to be deployed on embedded edge devices that require improved energy efficiency. For instance, the amazing performance of AlphaZero [8] required 4 to 6 weeks of training executed on 2,000 CPUs and 250 GPUs for a total of about 600KWh of power consumption (while the human brain of a Go player requires about 20W). Recent work [10] analyzing the carbon footprint of current natural-language processing models shows an alarming trend: training one huge Transformer model [2] for machine translation emits the same amount of CO2 as five cars in their lifetimes (fuel included). Such taxing demands are pushing both industry and academia to concentrate on custom platforms for DL algorithms that target improved performance and/or energy efficiency.

One general way to increase the performance and efficiency in computing is through reducing the numerical precision of basic arithmetic operations. In the case of DL systems, there are two main computational tasks: training and inference. Training requires vast quantities of labelled data that are used to optimize the network for the task at hand, usually by way of some form of stochastic gradient descent (SGD) algorithm. Inference, on the other hand, is the actual application of the trained network, which can be replicated onto millions of devices. Between the two, reducing numerical precision during inference has received the most attention from the research community over the last years, with some promising results in certain applications [11][13]. Much less has been done for the training phase, the main reason being that the effects of low-precision arithmetic on training algorithms are not yet well understood. This has by no means stopped major players in the hardware space to start devising architectures that offer increasing support for low-precision arithmetic. In the particular case of training, there are already commercial platforms that mix 32-bit high precision floating-point computing with low precision 16-bit formats for increased performance [4,8].

**Consignes pour postuler**

Please submit online: your resume, cover letter and letters of recommendation eventually.

For more information, please contact: silviu.filip@inria.fr, anastasia.volkova@univ-nantes.fr, olivier.sentieys@inria.fr

**Sécurité défense**

Ce poste est susceptible d’être affecté dans une zone à régime restrictif (ZRR), telle que définie dans le décret n°2011-1425 relatif à la protection du potentiel scientifique et technique de la nation (PPST). L’autorisation d’accès à une zone est délivrée par le chef d’établissement, après avis ministériel favorable, tel que défini dans l’arrêté du 03 juillet 2012, relatif à la PPST. Un avis ministériel défavorable pour un poste affecté dans une ZRR aurait pour conséquence l’annulation du recrutement.

**Politique de recrutement**

Dans le cadre de sa politique diversité, tous les postes Inria sont accessibles aux personnes en situation de handicap.

Attention: Les candidatures doivent être déposées en ligne sur le site Inria. Le traitement des candidatures adressées par d’autres canaux n’est pas garanti.
floating-point arithmetic formats and how the working precision can be effectively varied in-between training iterations. The student will also have the task of validating the developed techniques through a prototype of an accelerator for CNN training in the context of a collaboration with other researchers in the team.

References


Compétences

The student is expected to develop techniques for the mathematical formulation of quantization and compression models in deep neural networks, and energy-efficient hardware accelerators for machine learning applications. We also expect to have implementations of the developed techniques into a hardware accelerator developed as an FPGA prototype. The designs will primarily be done through High-Level Synthesis tools from C/C++. Ideal candidates should possess the following skills:

- Programming experience in C/C++ and Python.
- Good knowledge of computer architecture, computer arithmetic, hardware design, and embedded systems.
- Good knowledge of deep neural networks and deep learning.
- Experience with hardware acceleration on FPGA boards (especially Xilinx Zynq) would be a plus.
- Experience with deep learning frameworks (especially Pytorch) would be a plus.
- Basic knowledge in linear algebra, optimization, numerical computing, and machine learning in general.

Mostly importantly, we seek highly motivated and active students. A master in Computer Science, Computer Engineering, or Electronics Engineering is required.

Avantages

- Subsidised catering service
- Partially-reimbursed public transport

Rémunération

PhD student: monthly gross salary amounting to 1982 euros for the first and second years and 2085 euros for the third year