2020-03163 - Post-Doctoral Research Visit F/M Run-time management of safe-critical systems on multiprocessing platforms

Contrat renouvelable : Oui
Niveau de diplôme exigé : Thèse ou équivalent
Fonction : Post-Doctorant

A propos du centre ou de la direction fonctionnelle

The Inria Rennes - Bretagne Atlantique Centre is one of Inria’s eight centres and has more than thirty research teams. The Inria Center is a major and recognized player in the field of digital sciences. It is at the heart of a rich R&D and innovation ecosystem: highly innovative SMEs, large industrial groups, competitiveness clusters, research and higher education players, laboratories of excellence, technological research institutes, etc.

Contexte et atouts du poste

Social advantages
- Subsidised catering service
- Partially-reimbursed public transport
- Social security
- Paid leave
- Flexible working hours
- Sports facilities

Salary - Duration
- 18 months contract
- Monthly net salary amounting to ~2160 euros

Mission confiée

Context

The embedded systems from the safety-critical domain industries, such as the avionics, automotive, space, healthcare or robotics industries, face exponential growth in terms of performance requirements, while they have to deal with strict hard real-time constraints. This constantly growing processing demand has led the processor manufacturing industry towards multi- /many-core architectures. These architectures have multiple processor elements, called cores, providing massive computing power by concurrently executing a high volume of tasks. While such architectures can successfully meet the demands for the majority of computing systems, the same cannot be argued for hard real-time systems [1, 2]. Hard real-time systems have to provide timing guarantees in order to be safe, i.e. guarantee that tasks are completed before their respective deadlines and/or the total execution does not exceed a given latency requirement. Typical examples of such safety-critical systems is the Automatic Braking System (ABS) in automotive and the Fly-by-Wire control system in avionics.

In order to rigorously provide such guarantees, application deployment approaches, i.e. task mapping /scheduling, are based on the a priori knowledge of worst-case execution time (WCET) of tasks. There is a plethora of research in WCET estimation for uni-processor systems (see [2] for a review). However, in multi-core architectures, several arbitrated resources are shared among the cores (memory, interconnects, etc.) introducing timing delays and changing the timing behavior in a non-deterministic way. Thus, the WCET varies according to the task deployment, as tasks interfere when simultaneously access the on-chip shared resources. As a result, timing analysis and deployment optimisation for multicore systems becomes very challenging [3, 4, 5, 6, 7, 8]. This effect is particularly apparent in data-parallelizable applications, due to extensive resource sharing. We have observed that the WCET of tasks including interferences can be 750% times larger than the corresponding estimations without interferences [8] [9]. In order to unify the uni-processor deployment approaches to multi-processor architectures, the WCET of the tasks has to be over-approximated, so as to account for all possible interferences. This over-approximation practice has lead to the "one-out-of-m processors" problem [1] where the additional processing capacity is negated by the pessimism of the WCET. As a result, the sequential execution (on a single core) potentially provides better timing guarantees than any parallel execution, which seriously undermines the advantages of utilizing multi-cores. Nevertheless, recent state-of-the-art research [10] has shown that context-dependent WCETs, called interference-sensitive WCET (isWCET), reduce the pessimism in WCET leading to more efficient deployments on multi-core architectures.

In this work, we explore mechanisms to provide adaptation of the execution of the safety-critical systems so as to improve the actual run-time system performance, while still meeting the real-time constraints. This performance improvement allows the systems to provide higher Quality-of-Services constraints. This performance improvement allows the systems to provide higher Quality-of-Services guarantees in order to be safe, i.e. guarantee that tasks are completed before their respective deadlines and/or the total execution does not exceed a given latency requirement. Typical examples of such safety-critical systems is the Automatic Braking System (ABS) in automotive and the Fly-by-Wire control system in avionics.

References


Compétences
- PhD or Master in Computer Science, Electrical or Computer Engineering
- Programming experience, e.g., C/C++ language, HDL languages is a plus
- Computer architecture, hardware design, embedded software development, embedded systems
- Most importantly, we seek highly motivated and active researchers.

Avantages
- Subsidized meals
- Partial reimbursement of public transport costs

Rémunération
monthly gross salary amounting to 2653 euros