Offer #2022-04368

PhD Position F/M Time-guaranteed and reliable execution for safety-critical multicore systems

Contract type : Fixed-term contract

Level of qualifications required : Graduate degree or equivalent

Fonction : PhD Position

About the research centre or Inria department

The Inria Rennes - Bretagne Atlantique Center is one of Inria's eight centers and has more than thirty research teams. The Inria Center is a major and recognized player in the field of digital sciences. It is at the heart of a rich R&D and innovation ecosystem: highly innovative PMEs, large industrial groups, competitiveness clusters, research and higher education players, laboratories of excellence, technological research institute, etc.

Assignment

Thesis Context

The safety-critical embedded industries, such as avionics, automobile, robotics and health-care, require guarantees for hard real-time and correct application execution. As applications become more complex, their computational demands scale rapidly, requiring architectures with multiple processing elements. Although multicore architectures can effectively satisfy the needs of best-effort systems, the same cannot be stated for critical embedded systems due to hard-to-predict timing behaviour and increased fault susceptibility [1].

Hard-to-predict timing behaviour originates from the complex nature of modern systems. Not only application complexity, but also hardware complexity has been increased. Modern architectures are enhanced with dynamic hardware components with variable timing behaviour, while parallel execution of applications on the same platform leads to concurrent accesses to shared resources affecting applications' timing behaviour. To provide hard real-time guarantees, safe, but pessimistic, Worst-Case Execution Time (WCET) estimations have to be employed during system design [2]. Increased fault susceptibility stems from the nature of electronic systems. Reliability threats, such as manufacturing process variation, aging and soft errors, depend on transistors size and are expected to significantly increase with transistors shrinking [3]. Due to this unreliable nature of electronic systems, the susceptibility of multicore architectures towards reliability threats is inevitable [4]. However, the majority of existing WCET estimation approaches is fault-unaware; the hardware of the target platform is assumed to be fault-free [5]. As reliability issues become imminent due to technology scaling, such fault-unaware approaches become unsafe. With the technology size reduction, faults in combinational logic and smaller sequential logic of cores cannot be considered negligible anymore [6].

Thesis Goal

The goal of this PhD thesis is to provide the means to analyse both functional and timing behaviour of applications, perform fault-aware WCET estimation and design cores with timing guarantees and reliable execution. This will be achieved through novel approaches considering both reliability and WCET aspects. More precisely, a realistic and accurate functional and timing architectural vulnerability analysis will be proposed. This framework will be extended with probabilistic/hybrid WCET estimation techniques to provide fault-aware WCET estimations. Low-level fault-tolerant mechanisms will be designed to mitigate the most important impact of faults. The thesis will be based on open-source cores, e.g., RISC-V [7].

Bibliography

[1] S. Saidi, R. Ernst, S. Uhrig, H. Theiling, B. Dinechin, The Shift to Multicores in Real-Time and Safety-Critical Systems, in CODES + ISSS, p. 220-229, October 2015.

[2] C. Maiza. H. Rihani, J. Rivas, J. Goossens, S. Altmeyer, R. Davis, A Survey of Timing Verification Techniques for Multi-Core Real-Time Systems, ACM CS, 52(3):56:1-56:38, June 2019.

[3] P. Shivakumar, M. Kistler, S. Keckler, D. Burger, L. Alvisi, Modelling the effect of technology trends on soft error rate of combinational logic, in DSN, p. 389-398, June 2002

[4] S. Rehman, M. Shafique, J. Henkel, Reliable Software for Unreliable Hardware: A Cross Layer Perspective, Springer, 2016.

[5] A. Lofwenmark, S. Nadjm-Tehrani, Fault and timing analysis in critical multi-core systems: A survey with an avionics perspective, JSA, vol. 87, p. 1-11, 2018

[6] N. Mahatme S. Jagannathan, T. Loveless, L. Massengill, B. Bhuva, S. Wen, R. Wong, Comparison of Combinational and Sequential Error Rates for a Deep Submicron Process, IEEE NS, vol. 58, p. 2719–2725, Dec. 2011

[7] S. Rokicki, D. Pala, J. Paturel, and O. Sentieys. What You Simulate Is What You Synthesize: Designing a Processor Core from C++ Specifications, in International Conference on Computer-Aided Design (ICCAD), pages 1–8, Nov. 2019.

Skills

Required expertise

- Good knowledge of computer architecture, embedded systems and real-time systems
- Mathematical methods and probabilities
- Working experience in the areas of Worst Case Execution Time and fault tolerance is an advantage
- Programming experience in C/C++ and python
- Familiarity with FPGA design and/or High-Level Synthesis.

A master in Computer Science, Computer Engineering, or Electrical Engineering is required. An equivalent engineering degree (5th year) enabling to start doctoral studies is also accepted.

Languages and skills:

- Very good communication skills in oral and written English.
- Open-mindedness, strong integration skills and team spirit.
- Mostly importantly, we seek highly motivated people.

Please send:

- Your CV along with your Bachelor/Master transcripts
- A motivational letter
- Reference letters
- Any additional documents/links that you think can show your experience (reports, notes, papers, github repositories...)

Benefits package

- Subsidized meals
- Partial reimbursement of public transport costs

Remuneration

Monthly gross salary amounting to 1982 euros for the first and second years and 2085 euros for the third year

General Information

- **Theme/Domain :** Architecture, Languages and Compilation
  System & Networks (BAP E)
- **Town/city :** Rennes
- **Inria Center :** Centre Inria de l'Université de Rennes
- **Starting date :** 2022-03-01
- **Duration of contract :** 3 years
- **Deadline to apply :** 2022-06-30

Contacts

- **Inria Team :** TARAN
- **PhD Supervisor :**
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About Inria

Inria is the French national research institute dedicated to digital science and technology. It employs 2,600 people. Its 200 agile project teams, generally run jointly with academic partners, include more than 3,500 scientists and engineers working to meet the challenges of digital technology, often at the interface with other disciplines. The Institute also employs numerous talents in over forty different professions. 900 research support staff contribute to the preparation and development of scientific and entrepreneurial projects that have a worldwide impact.

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Please submit online : your resume, cover letter and letters of recommendation eventually

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Defence Security :
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST).Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy :
As part of its diversity policy, all Inria positions are accessible to people with disabilities.