Offer #2023-06475

Post-Doctoral Research Visit F/M Analysis and design of reliable domain-specific processors

Contract type: Fixed-term contract

Renewable contract: Yes

Level of qualifications required: PhD or equivalent

Function: Post-Doctoral Research Visit

About the research centre or Inria department

The Inria Rennes - Bretagne Atlantique Centre is one of Inria's eight centres and has more than thirty research teams. The Inria Center is a major and recognized player in the field of digital sciences. It is at the heart of a rich R&D and innovation ecosystem: highly innovative PMEs, large industrial groups, competitiveness clusters, research and higher education players, laboratories of excellence, technological research institute, etc.

Context

Host team: The project will be held in the TARAN (formerly CAIRN) team of the IRISA/INRIA laboratory. The TARAN team, with more than 35 members from Inria, URI, and ENS Rennes, has participated in several national and European R&D projects (H2020 ARG0, FP7 Alma, FP7 Flextiles) and has strong industrial collaborations (e.g., Safran, Thales, Alcatel, Orange, STMicroelectronics, Technicolor, and various SMEs). TARAN has recognized experience in several domains related to the project, such as embedded system design, fault tolerance, safety-critical systems, computing architectures, design tools for specialized hardware architectures.

Acquiring new skills: As a new member of the TARAN team, you will be integrated in a research group with excellent prestige and deep knowledge of embedded systems. The TARAN research group can provide you with a more solid understanding and knowledge of computer architectures and hardware design. For instance, the host team has high-quality papers published in reliability and fault tolerance, using RISC-V-based processors and dedicated hardware designs, subjects that you will be able to learn much more about and increase my background in this area.

Assignment

Context: The dense transistor integration on the silicon and the systems architecture complexity have increased the system sensitivity to faults. Since the 1980s it is known that the terrestrial cosmic rays cause several defects in electronic components, from logical faults up to the circuit destruction. The occurrences of this phenomenon, called SEE (Single Event Effect), have significantly increased in the 90s due to the downscaling of the transistor technology and the increase in the memory sizes. Up to now, most of the mitigation solutions have focused on the Single-Event Upsets (SEUs), as they have been identified as the dominant issue. The Single-Event Transients (SETs) were not considered as a major problem, because of digital logic characteristics, such as logic masking, electrical masking and locking. However, as the transistor sizes, capacitances and supply voltages decrease, the threshold required for a transient impulse to disturb the circuit has become increasingly low. Combined with the high operating frequencies, the possibility that a SET in the combinational logic will be stored on the storage element is increased. Therefore, SETs will rapidly exceed the SEU error rate in integrated systems, whereas the probabilities for multiple faults (Multiple-Bit Upset - MBU) are highly increased.

To deal with these problems, the architectures must have mechanisms to detect faults and to remedy their impacts on the application. However, to select an efficient error detection and correction mechanism, the potential faults and their impacts on the processor are required to be analyzed in order to drive the design of fault tolerant mechanisms removing the unnecessary performance, area and energy overhead.

Main activities

Goal: The topic of this position is to study the behavior of the domain-specific processors under the presence of faults, develop error models in higher abstract layers that the existing ones at the transistor level, and propose effective protection mechanisms across different design layers.

To achieve this goal, we will develop a cross-layer framework to perform vulnerability analysis through fault injection methodologies applied at different system layers. The methodology should decide
where to insert faults in order to have a realistic simulation of the radiation impact on the processor components, whereas the development should take into account how to avoid exhaustive exploration in order to reduce the time of the experiments. As a first step, the fault injection methodology will be based on scripts that modify the processor's component by inserting faults at the gate level. The experiments can be performed by configuring adequately each time the fault injection occurs. The results gather from the experiments will be used to obtain information to develop error higher abstraction models at the architecture level and to characterize the sensibility of the different components of the processor to transient errors and drive the protection mechanisms.

**Skills**

**Required expertise**

- Good knowledge of computer architecture, hardware and embedded systems
- Good knowledge with FPGA design and/or High-Level Synthesis.
- Programming experience in HDL, tcl, bash scripting, C/C++ and python

A Phd in Computer Science, Computer Engineering, or Electrical Engineering is required.

Note that we also receive applications on the same topic for an engineering position (master is required).

**Languages and skills:**

- Very good communication skills in oral and written English.
- Open-mindedness, strong integration skills and team spirit.
- Most importantly, we seek highly motivated people.

**Please send:**

- Your CV along with your Bachelor/Master transcripts
- A motivational letter
- Reference letters
- Any additional documents/links that you think can show your experience (reports, notes, papers, github repositories...)

**Benefits package**

- Subsidized meals
- Partial reimbursement of public transport costs
- Possibility of teleworking (90 days per year) and flexible organization of working hours
- Partial payment of insurance costs

**Remuneration**

Monthly gross salary amounting to 2746 euros

**General Information**

- **Theme/Domain:** Architecture, Languages and Compilation System & Networks (BAP E)
- **Town/city:** Rennes
- **Inria Center:** Centre Inria de l'Université de Rennes
- **Starting date:** 2023-09-01
- **Duration of contract:** 1 year
- **Deadline to apply:** 2023-12-31

**Contacts**

- **Inria Team:** TARAN
- **Recruiter:** Kritikakou Angeliki / angeliki.kritikakou@irisa.fr

**About Inria**

Inria is the French national research institute dedicated to digital science and technology. It employs 2,600 people. Its 200 agile project teams, generally run jointly with academic partners, include more than 3,500 scientists and engineers working to meet the challenges of digital technology, often at the interface with other disciplines. The Institute also employs numerous talents in over forty different professions. 900 research support staff contribute to the preparation and development of scientific and entrepreneurial projects that have a worldwide impact.

**Warning:** you must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.
Instruction to apply

Please submit online: your resume, cover letter and letters of recommendation eventually

For more information, please contact angeliki.kritikakou@irisa.fr

Defence Security:
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST). Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy:
As part of its diversity policy, all Inria positions are accessible to people with disabilities.