The topic of this position is to study the behavior of the domain-specific processors under the presence of faults, develop error models in higher abstract layers that the existing ones at the transistor level, and propose effective protection mechanisms across different design layers.

To achieve this goal, we will develop a cross-layer framework to perform vulnerability analysis through fault injection methodologies applied at different system layers. The methodology should consider the insertion of faults, a realistic simulation of the radiation impact on the processor components, whereas the development should take into account how to avoid exhaustive exploration in order to reduce the time of the experiments. As a first step, the fault injection methodology will be based on scripts that the transistor technology and the increase in the memory sizes. Up to now, most of the SEUs, have significantly increased in the 90s due to the downscaling of SEE (Single Event Effect), have significantly increased in the 90s due to the downscaling of the transistor technology and the increase in the memory sizes. Up to now, most of the mitigation solutions have focused on the Single-Event Upsets (SEUs), as they have highly increased.

Mission confiée
Context: The dense transistor integration on the silicon and the systems architecture complexity have increased the system sensitivity to faults. Since the 1980s it is known that the terrestrial cosmic rays cause several defects in electronic components, from logical faults up to the circuit destruction. The occurrences of this phenomenon, called SEE (Single Event Effect), have significantly increased in the 90s due to the downscaling of the transistor technology and the increase in the memory sizes. Up to now, most of the mitigation solutions have focused on the Single-Event Upsets (SEUs), as they have been identified as the dominant issue. The Single-Event Transients (SETs) were not considered as a major problem, because of digital logic characteristics, such as logic masking, electrical masking and locking. However, as the transistor sizes, capacitances and supply voltages decrease, the threshold required for a transient impulse to disturb the circuit has become increasingly low. Combined with the high operating frequencies, the possibility that a SET in the combinational logic will be stored on the storage element is increased. Therefore, SETs will rapidly exceed the SEU error rate in integrated systems, whereas the probabilities for multiple faults (Multiple-Bit Upset - MBU) are highly increased.

To deal with these problems, the architectures must have mechanisms to detect faults and to remedy their impacts on the application. However, to select an efficient error detection and correction mechanism, the potential faults and their impacts on the processor are required to be analyzed in order to drive the design of fault tolerant mechanisms removing the unnecessary performance, area and energy overhead.

Principales activités
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Compétences

Required expertise
- Good knowledge of computer architecture, hardware and embedded systems
- Good knowledge with FPGA design and/or High-Level Synthesis.
- Programming experience in HDL, tcl, bash scripting, C/C++ and python

A PhD in Computer Science, Computer Engineering, or Electrical Engineering is required.

Note that we also receive applications on the same topic for an engineering position (master is required).

Languages and skills:
- Very good communication skills in oral and written English.
- Open-mindedness, strong integration skills and team spirit.
- Mostly importantly, we seek highly motivated people.

Please send:
- Your CV along with your Bachelor/Master transcripts
- A motivational letter
- Reference letters
- Any additional documents/links that you think can show your experience (reports, notes, papers, github repositories...)

Avantages

- Subsidized meals
- Partial reimbursement of public transport costs
- Possibility of teleworking (90 days per year) and flexible organization of working hours
- Partial payment of insurance costs

Rémunération

monthly gross salary amounting to 2746 euros